Client's ref.: MXIC IDF200112372/王俊淇
File: 0389-7513USF/Jacky/Kevin

TITLE

METHOD OF FORMING JUNCTION ISOLATION TO ISOLATE ACTIVE ELEMENTS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the semiconductor manufacturing process, and more particularly, to a method of forming junction isolation to isolate active elements.

Description of the Related Art

All non-trivial integrated electronics involve connection of isolated devices through specific electrical connection paths. The device isolation scheme is therefore critical when fabricating integrated circuits.

Shallow and deep trench isolations have been introduced to the fabrication of devices for isolation between device elements. The trenches are formed by removing part of a silicon substrate with dry etching. Then, using deposition, dielectric material is filled in the trenches, and the surface profile of the trenches is planarized by CMP (chemical mechanical polishing).

Depending on the etching process, refilling process and CMP steps, the fabrication has some drawbacks. For instance, the manufacturing process is complex and costly. In addition, voids are easily formed in the trench during deposition. Also, crystal defects such as dislocation inevitably occur during the trench process. Such defects seriously affect device reliability and yield.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a method of forming junction isolation in a semiconductor substrate.

Another object of the present invention is to provide a method of forming junction isolation to isolate active elements.

In order to achieve these objects, a method of forming junction isolation to isolate active elements is provided. A semiconductor substrate having a plurality of active areas and an isolation area between active areas is provided. A first gate structure is formed on part of the substrate located in the active areas and, simultaneously, a second gate structure serving as a dummy gate structure is formed on the substrate located in the isolation area. A first doped region is formed in the substrate located at two sides of the first gate structure and two sides of the second gate structure. A bottom anti-reflection layer is formed on the substrate, the first gate structure and the second gate structure. Using anisotropy etching, part of the bottom anti-reflection layer is etched back to expose the second gate structure. The second gate structure is removed to expose the substrate. A second doped region serving a junction isolation region is formed in the substrate located in the isolation area. The bottom anti-reflection layer is removed.

The present invention improves on the prior art in that the present method uses the self-alignment of the gate structures to define the isolation area and the active area. Then, after removing the dummy gate structure, suitable ions are implanted into the substrate located in the isolation area to form a junction isolation region in the substrate. Thus, the invention can avoid voids and defects in the substrate, thereby raising reliability and yield, and ameliorating the disadvantages of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

Figs. 1~6 are sectional views according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figs. 1~6 are sectional views according to an embodiment of the present invention.

In Fig. 1, a semiconductor substrate 100 having a plurality of predetermined active areas 110 and at least one predetermined isolation area 120 between any two active areas 110 is provided. In principle, any semiconductor substrate can be processed using the isolation technique of the invention. In the most likely commercial embodiment, the substrate 100 will be silicon.

In Fig. 1, a first gate structure 130 is formed on part of the substrate 100 located in each of the active areas 110, and a second gate structure 140 is formed on the substrate 100 located in the isolation area 120. As a demonstrative method of forming the first gate structure 130 and the second gate structure 140, referring to Fig. 1, an insulation layer (not shown), such as a SiO_2 layer, is formed on the substrate 100 by deposition or thermal oxidation. A conductive layer (not shown), such as a polysilicon layer, is formed on the insulation layer by deposition. Using anisotropy etching, part of the conductive layer and the insulation layer are etched back to form a gate layer 132 and a gate insulation layer 131 on the substrate 100 in each active areas 110 and isolation area 120. That is, the first gate

structure 130 and the second gate structure 140 can be simultaneously (in situ) formed on the substrate 100. In addition, the second gate structure 140 serves as a dummy gate structure and will be removed in subsequent process.

In Fig. 1, using implantation of first type ions, a first doped region 150 is formed in the substrate 100 located at two sides of the first gate structure 130 and two sides of the second gate structure 140. The first doped region 150 serves as a source or drain region. Thus, an active element having the first gate structure 130 and the first doped region 150 is obtained.

In Fig. 2, a bottom anti-reflection layer 210 is formed on the substrate 100, the first gate structure 130 and the second gate structure 140 by, for example, coating. The bottom anti-reflection layer 210 can be an organic layer, for example, model: AR2 produced by Shipley company.

In Fig. 2, using photolithography, a patterned photoresist layer 220 is formed on the bottom anti-reflection layer 210 located in the active areas 110.

In Fig. 3, using the patterned photoresist layer 220 as a mask, part of the bottom anti-reflection layer 210 is removed by anisotropy etching to expose the top surface of the second gate structure 140. The isotropic etching gas may be $HBr+O_2$.

In Fig. 4, the second gate structure 140 is removed by anisotropy etching to expose the surface of the substrate 100. The isotropic etching gas may be $CCl_4+HBr+O_2$.

In Fig. 5, using the patterned photoresist layer 220 and the remaining bottom anti-reflection layer 210 as a mask, a second doped region 520 is formed in the substrate 100 located in the isolation area 120 by, for example, implantation 510 of second

type ions. The conditions of the implantation 510 can be 40~80 KeV for power and 1E18~1E19 cm^{-3} for dosage.

It should be noted that the first type ions and the second type ions are different. When the first type ions are N-type ions, the second type ions are P-type ions. Contrarily, when the first type ions are P-type ions, the second type ions are N-type ions. The N-type ions are, for example, phosphorous ions or arsenic ions. The P-type ions are, for example, boron ions. Thus, according to the above steps, the second doping region 520 serving as a P-N junction isolation region to isolate active elements is obtained.

In Fig. 6, the patterned photoresist layer 220 is removed by wet or dry etching.

In Fig. 6, the bottom anti-reflection layer 210 is removed by wet or dry etching.

Thus, the present invention uses the self-alignment of the gate structures to define the isolation area and the active area, then removes the dummy gate structure, and then implants suitable ions into the substrate located in the isolation area to form junction isolation. Thus, the invention avoids voids and defects existing in the substrate, thereby raising reliability and yield, and ameliorating the disadvantages of the prior art.

Finally, while the invention has been described by way of example and in terms of the above, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.